REMARKS

Claims 5, 8, 10, 11, 33, 47, 48, 53, 54, 70, 71, 74 and 75 are pending, with claims 5, 8 and 70 being independent. By this amendment, 5, 8, 10, 33, 70, and 71 have been amended, and claims 37 and 72 have been canceled. No new matter has been introduced.

With respect to the objection to the drawings, applicant notes that the recitation in claim 33 that "said memory circuits and said D/A converter are arranged so as to overlap a source signal line" is supported by FIG. 30, which shows memory circuits 3302-3304 and D/A converter 3305 overlapping with source signal line 3307. Accordingly, for at least this reason, applicant requests withdrawal of this objection.

For the same reasons, applicant requests reconsideration and withdrawal of the rejection of claims 33 and 71 under 35 U.S.C. 112, first paragraph, for alleged failure of the specification to comply with the written description requirement. In particular, the specification supports the recitation from claims 33 and 71 that the memory circuits and the D/A converter are arranged so as to overlap a source signal line at Fig. 30 and page 41, lines 15-16.

Applicant requests reconsideration and withdrawal of the rejection of claim 5 under section 112, second paragraph, in view of the amendments to claim 5. In particular, claim 5 has been amended to recite that the memory circuits, rather than the pixels, store the digital signals.

Claims 5, 8, 33, 47, 48, 53, 54, 70-72, 74 and 75 have been rejected as being unpatentable over Okumura (U.S. Patent No. 5,945,972). With respect to claims 5 and 70, and their dependent claims, applicant requests reconsideration and withdrawal of this rejection because Okumura does not describe or suggest having a pixel include a source signal line and n TFTs connected to the source signal line, as recited in claims 5 and 70, and shown in Fig. 1. Rather, Okumura, at col. 21, lines 8-13 and Figs. 14 and 17, describes an arrangement in which the source of SW1 is connected to a signal line 301 and the memory circuit 321 is connected between the drain of SW1 and the source of SW2. Okumura simply does not describe or suggest having a pixel include TFTs connected to the source signal line. Accordingly, the rejection should be withdrawn.

With respect to claim 8 and its dependent claims, applicant requests reconsideration and withdrawal of this rejection because Okumura does not describe or suggest having a pixel include a source signal line and n TFTs connected to the source signal line and to an input terminal of a memory circuit, as recited in claim 8. Rather, as noted above, Okumura, at col. 21, lines 8-13 and Figs. 14 and 17, describes an arrangement in which the source of SW1 is connected to a signal line 301 and the memory circuit 321 is connected between the drain of SW1 and the source of SW2. Okumura simply does not describe or suggest having a pixel include TFTs connected to the source signal line and to memory circuits. Accordingly, the rejection should be withdrawn.

Claims 10 and 11 have been rejected as being unpatentable over Okumura in view of Nagao (U.S. Patent No. 6,380,876). Applicant requests reconsideration and withdrawal of this rejection because Nagao does not remedy the failure of Okumura to describe or suggest the subject matter of claim 8 from which claims 10 and 11 depend.

Applicant submits that all claims are in condition for allowance.

No fees are believed to be due. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 7/19/05

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